ENGINEERING RESOURCE

High-Speed FPGA Interface Design Review Checklist

A structured review aid for source-synchronous, differential, parallel, and converter-to-FPGA interfaces.

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Use	Project preparation and technical review

This resource is a practical starting point, not a substitute for device documentation, project-specific engineering analysis, safety review, regulatory assessment, or formal certification.

01 | SYSTEM DEFINITION

Requirements and interface inventory

Complete this page before approving connector selection, FPGA pins, or PCB routing.

CHECK	REVIEW ITEM	NOTES / EVIDENCE
[ ]	The interface purpose, endpoints, operating modes, and required availability are defined.	
[ ]	Data width, channel count, sample or transfer rate, edge rate, and sustained throughput are recorded.	
[ ]	Every signal is classified by direction, voltage standard, clock relationship, and termination.	
[ ]	Differential pairs, forwarded clocks, reference clocks, resets, control signals, and power rails are listed.	
[ ]	Startup, reset, training, alignment, re-alignment, and fault-recovery behavior are defined.	
[ ]	Backpressure, buffering, trigger latency, burst length, and host-service assumptions are quantified.	
[ ]	Connector variant, mating part, keying, pin numbering, keep-out, and mounting constraints are verified.	
[ ]	A controlled pin-mapping record exists and identifies polarity, grounds, reserved pins, and no-connects.	
[ ]	The interface owner and approval status are identified for both endpoints.	

Review outcome: [ ] Approved [ ] Approved with actions [ ] Rework required

02 | HARDWARE

PCB, clocking, power, and mechanics

CHECK	REVIEW ITEM	NOTES / EVIDENCE
[ ]	The PCB stack-up is confirmed with the fabricator and controlled-impedance geometry is calculated from it.	
[ ]	Differential impedance, single-ended impedance, termination, and allowable discontinuities are specified.	
[ ]	Pair symmetry, spacing, maximum route length, stubs, vias, and connector transitions are reviewed.	
[ ]	Reference-plane continuity and return-current paths are maintained across the full interconnect.	
[ ]	FPGA I/O-bank voltage and the remote device's electrical standard are compatible in every mode.	
[ ]	Clock source, jitter requirement, distribution, termination, phase relationship, and measurement access are defined.	
[ ]	Power rails, sequencing, current estimates, regulator stability, decoupling, and test points are reviewed.	
[ ]	ESD, overvoltage, hot-plug, isolation, and protection requirements are addressed where applicable.	
[ ]	Connector orientation, board outline, mounting, height, airflow, enclosure, and cable strain are checked.	
[ ]	Schematic symbols, footprints, pin numbers, polarity marks, and assembly orientation are independently reviewed.	

03 | FPGA

Pins, capture architecture, constraints, and CDC

CHECK	REVIEW ITEM	NOTES / EVIDENCE
[ ]	Pin assignment is checked against the exact FPGA package, I/O bank, differential capability, and clock resources.	
[ ]	A small pin-planning compile confirms legal placement, I/O standards, and required device resources.	
[ ]	The capture clock, frame signal, data lanes, processing clock, and host clock are explicit in the architecture.	
[ ]	Input capture uses appropriate I/O, DDR, SERDES, delay, and clock-network resources.	
[ ]	Bit order, polarity, word width, framing, channel grouping, and valid signaling are documented.	
[ ]	Generated clocks, input delays, clock relationships, and asynchronous paths reflect the physical interface.	
[ ]	Clock-domain crossings use reviewed structures; reset release and data coherence are verified.	
[ ]	FIFO depth covers worst-case clock ratio, burst, trigger, and host-stall behavior with margin.	
[ ]	Alignment status, error counters, FIFO levels, build ID, and triggerable debug capture are available.	
[ ]	Simulation covers normal traffic, reset, framing errors, polarity/bit-order faults, overflow, and recovery.	

04 | VERIFICATION

Bring-up, evidence, and controlled release

CHECK	REVIEW ITEM	NOTES / EVIDENCE
[ ]	A safe bring-up sequence defines inspection, current limits, expected rails, clock checks, and stop conditions.	
[ ]	Known digital test patterns or loopback modes isolate link alignment from analog or application behavior.	
[ ]	One lane or channel is verified before expansion to the complete interface.	
[ ]	Known stimulus is correlated across laboratory instruments, FPGA capture, firmware, and host data.	
[ ]	Timing reports and device configuration are preserved with the tested programmable image.	
[ ]	Repeated startup, reset recovery, configuration changes, triggers, long-duration traffic, and host stalls are tested.	
[ ]	Overflow, underflow, loss-of-lock, and transport errors are observable and included in acceptance testing.	
[ ]	Test evidence records hardware, FPGA, firmware, software, procedure, equipment, and configuration revisions.	
[ ]	Open issues, limitations, deviations, corrective actions, and re-verification status are documented.	
[ ]	The release package contains approved source, constraints, generated artifacts, instructions, and evidence index.	

Final decision: [ ] Release [ ] Conditional release [ ] Hold

Reviewer: _____ Date: _____ Release ID: _____